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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KEVIN M. CHRISTIANSEN

Appeal 2009-2719
Application 10/667,241
Patent 5,961,614
Technology Center 2100

Decided:[1] March 20, 2009

Before HOWARD B. BLANKENSHIP, SCOTT R. BOALICK, and KEVIN F. TURNER, *Administrative Patent Judges.*

TURNER, *Administrative Patent Judge*

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134 from the Final Rejection of claims 21-36. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF THE CASE

This proceeding arose from a reissue request filed by Appellant, with consent of all assignees, on September 18, 2003 for United States Patent 5,961,614 issued to Kevin M. Christiansen (Appellant) on October 5, 1999, based on United States Application 08/647,451, filed May 7, 1996. The United States Application, which matured into the subject patent, was itself a continuation-in-part of United States Application 08/436,969, filed May 8, 1995, now abandoned. The present reissue application is a continuation of a prior reissue application, 09/972,847, filed October 4, 2001, now abandoned.

Appellant's invention relates to methods and systems for transferring data between a computer memory and an external system, where a controller uses information from an interfacing device to transfer the data more efficiently (Abstract).

Claims 1-36 are pending in the instant application, where claims 1-20 have been allowed and claims 21-36 stand finally rejected.

Claim 21, which we take to be representative, was added through amendment and reads as follows:

> 21. A memory access controller adapted to be coupled to a computer system memory and an Input/Output (I/O) device, comprising:
>
> a register that stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer; and

> circuitry coupled to the register that receives the data status signal and for controlling subsequent operation of the memory access controller based on the data status signal.

(App. Br. 11, Claims Appendix)

The prior art references relied upon by the Examiner in rejecting the claims is:

Kawai	5,584,010	Dec. 10, 1996
Matsumoto	5,614,685	Mar. 25, 1997

The Examiner rejected claims 21-36 under 35 U.S.C. § 103(a) as unpatentable over Kawai and Matsumoto (Ans. 3-8).

ISSUES

Appellant contends that the Examiner's rejection is in error because the combination of Kawai and Matsumoto fails to teach or suggest all of the limitations of the rejected claims (App. Br. 5). Appellant asserts that cited references fail to disclose or suggest "a register that stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer," "means for storing a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer system," or "a memory configured to store status data generated by an Input/Output (I/O) device after a data unit transfer between the computer system memory and a system external to the computer system" (*Id.*). Specifically, Appellant argues that references to

external elements in Kawai and Matsumoto refer merely to elements that are external to chip memory or chip DSP, but not external to the system, as required by the above claim elements (App. Br. 6-7). Appellant also argues that Matsumoto fails to disclose a register that stores a data status signal generated after the transfer of the data (App. Br. 7-8).

The Examiner responds that Matsumoto does not define the term "external," such that it should be given its plain meaning and that one of ordinary skill in the art would have understood that an external device or system would be external to the computer system (Ans. 10). The Examiner also finds that Appellant's argument that Matsumoto fails to disclose a register as claimed overlooks the disclosure of Kawai, which provides such a register, and asserts that Appellant is arguing the references individually (Ans. 11-12).

Thus, the issues arising from the respective positions of Appellant and the Examiner are:

Has Appellant shown reversible error in the Examiner's determination that Kawai and Matsumoto suggest a data status signal generated by transfers of a data unit to a system external to the computer system?

Has Appellant shown reversible error in the Examiner's determination that Kawai and Matsumoto suggest a register that stores a data status signal generated after the transfer of the data?

FINDINGS OF FACT

1. Appellant's Specification discloses an integrated I/O controller which controls I/O devices, where each I/O device is in turn connected to an external device system. The I/O controller controls the flow of data from the I/O devices where the data can be stored in a memory. The memory includes a channel status register having status bits that are used for status and control of memory channels (Spec. col. 3, l. 45 – col. 4, l. 12; Fig. 1, elements 10, 20, 50, 90, 110).
2. Kawai discloses a digital signal processor (DSP) having a direct memory access control device coupled to an internal data memory and an input/output interface circuit. The direct memory access control device includes a control unit and a status register, where the status register stores a signal indicating destination specifying information and destination state information (Col. 7, l. 48 – col. 8, l. 51; Figs. 6 and 7, elements 100, 103, 108, 200, 251, 260).
3. Both Appellant and the Examiner acknowledge that Kawai fails to teach that the data unit is transferred to a system external to the computer (App. Br. 6; Ans. 4).
4. Matsumoto discloses a DSP which performs data processing on data stored in memory. The DSP is in communication with data RAM and includes a data input/output (I/O) control portion that

communicates through data busses (DB) (Abstract; Col. 3, ll. 2-22; Fig. 1, elements 3, 12, 14).

5. Matsumoto details the connection between the DSP and an external device or system in the following paragraph:

> The data R/W control portion 11 performs a data input/output control between the data RAM 14 and DSP 3. In order to do so, the data R/W control portion 11 outputs control signals to the data memory address control portion 10. In accordance with the instructions (i.e., control signals) from the control portion 8, the data I/O control portion 12 performs a data input/output control on data to be transmitted between the DSP 3 and the external device or system.

(Col. 3, ll. 60-67).

PRINCIPLES OF LAW

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 127 S. Ct. 1727, 1734 (2007).

KSR disapproved a rigid approach to obviousness (*i.e.*, an analysis *limited to* lack of teaching, suggestion, or motivation). *KSR*, 127 S. Ct. at 1741 ("The obviousness analysis cannot be confined by a formalistic

conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents.").

During examination, the claims must be interpreted as broadly as their terms reasonably allow. *In re Am. Acad. of Sci. Tech Center*, 367 F.3d 1359, 1369 (Fed. Cir. 2004). When the specification states the meaning that a term in the claim is intended to have, the claim is examined using that meaning, in order to achieve a complete exploration of the applicant's invention and its relation to the prior art. *In re Zletz*, 893 F.2d 319, 321-22 (Fed. Cir. 1989). "Even when guidance is not provided in explicit definitional format, the specification may define claim terms by implication such that the meaning may be found in or ascertained by a reading of the patent documents." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1321 (Fed. Cir. 2005) (citations and internal quotation marks omitted).

ANALYSIS

Appellant argues claims 21-36 together. We therefore select claim 21 as representative, and claims 22-36 stand or fall with claim 21. 37 C.F.R. § 41.37(c)(1)(vii).

Appellant argues that Matsumoto only uses the term "external device or system" once in its specification and implies that the external device or system is merely external to the DSP itself, and not external to the computer system (App. Br. 6; Reply Br. 2). The Examiner acknowledges that

Matsumoto does not explicitly define "external device or system," but finds that the term would have been understood according to its plain meaning by one of ordinary skill in the art. Such an understanding would be that the communication is made with a system or device external to the computer (Ans. 10). We agree with the Examiner. While Appellant espouses a narrow reading of the term "external device or system," we cannot say that one of ordinary skill in the art would necessarily take such a narrow reading. The fact that the term references not only a "device" but also a "system" external to the DSP, (FF 5), implies that it would not have been unreasonable for one of ordinary skill in the art to have interpreted communications with a system external to the computer system comprised of the DSP, memories, and the CPU. As such, we find no error in the Examiner's interpretation of the disclosure of Matsumoto.

In addition, Appellant argues that given Matsumoto's use of the term "external data memory," as being separate from the DSP but included in the same system, the use of the word "external" in Matsumoto merely describes a device off-chip (App. Br. 6-7). Appellant also argues that the use of the term "external device" in Kawai also supports Appellant's contention that an "external device" is external to the DSP yet internal to the computer (Reply Br. 3-4). While the use of "external," with respect to memory in Matsumoto may imply that the memory is merely off-chip, we do not find that use of the term in that manner implies that all other uses of "external" are also limited to off-chip. As the Examiner finds, Matsumoto teaches separate logic for

communicating with the RAM that does not use the I/O control portion, (Ans. 10), such that the use of the term "external" with respect to memory need not limit the implications of the term "external device or system." Additionally, while Appellant may be correct that Kawai uses "external device" to mean merely external to the DSP, we do not find that this overrides the plain meaning that one of ordinary skill in the art would apply to the term "external device or system" disclosed in Matsumoto.

Appellant also argues that Matsumoto fails to disclose a register that stores a data status signal generated after the transfer of the data to a system external to the computer (App. Br. 7-8). Appellant argues that Matsumoto fails to disclose storing information associated with the completion of a data transfer and Kawai only describes communication between DSPs within a single system (App. Br. 7-8). However, we agree with the Examiner that Appellant is arguing the references individually and not the combination (Ans. 11-12). Since Kawai discloses a storage device register that stores a data status signal generated by the I/O device after data transfer, (FF 2), assuming communication with an external system, as suggested by Matsumoto, a status signal would be stored upon data transfer in the combination. As such, we do not find error in the Examiner's rejection of claims 21-36.

CONCLUSIONS

Appellant has failed to show that the Examiner reversibly erred in determining that: (i) Kawai and Matsumoto suggest a data status signal generated by transfers of a data unit to a system external to the computer system; and (ii) Kawai and Matsumoto suggest a register that stores a data status signal generated after the transfer of the data.

DECISION

The decision of the Examiner rejecting claims 21-36 is AFFIRMED.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

rvb

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